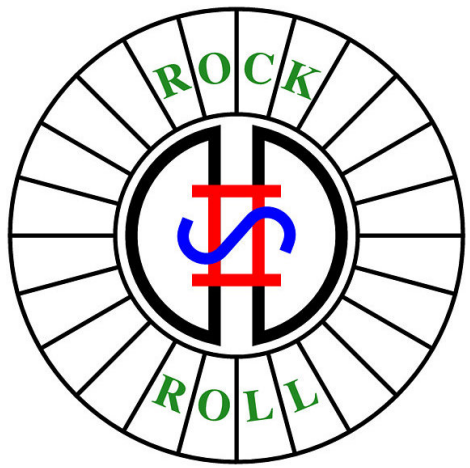
Greg Feild
Ace School
3/26/2004

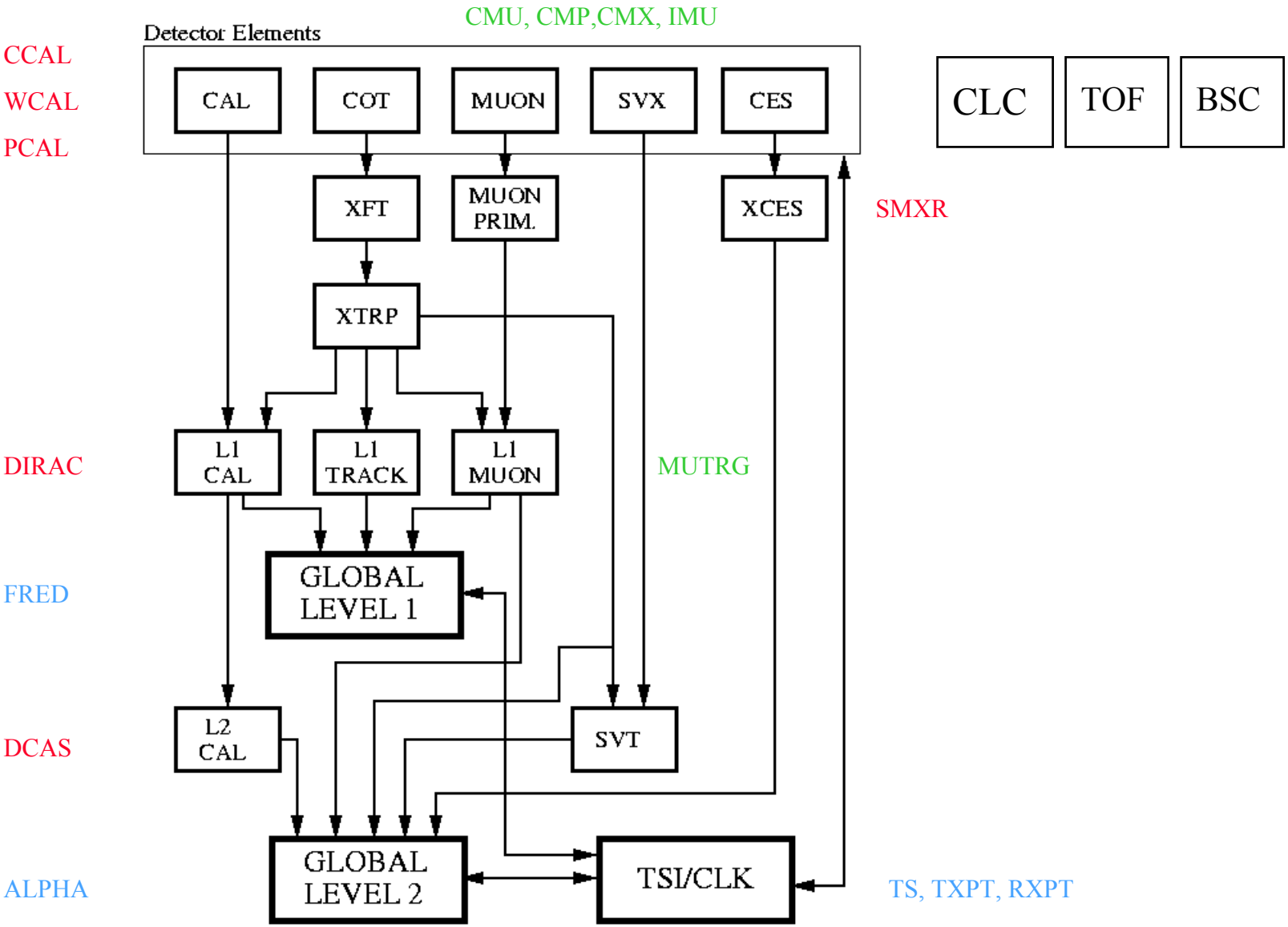
Triggers and Scalers

Greg Feild
Ace School
1/15/2004

Triggers and Scalers

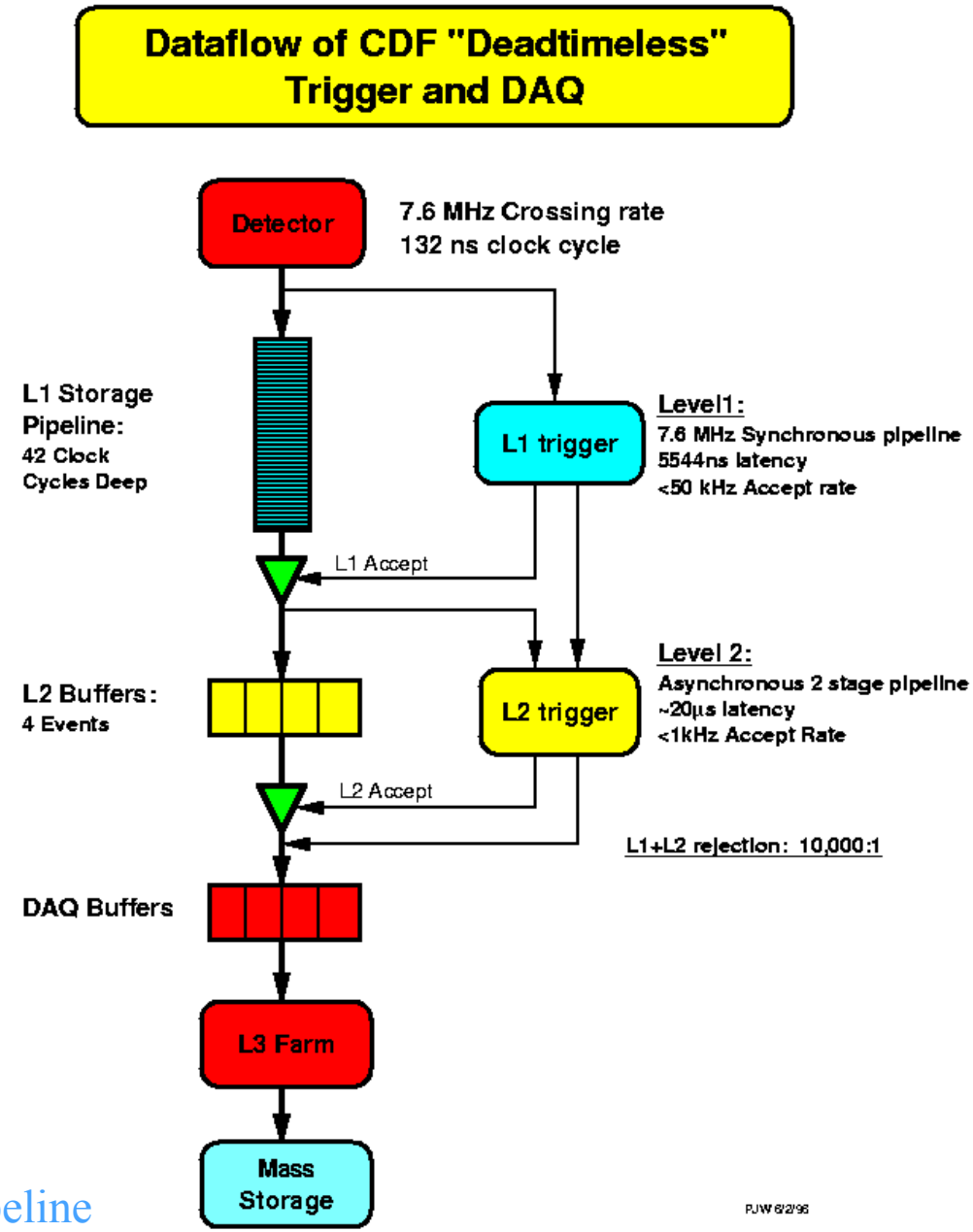


RUN II TRIGGER SYSTEM



Trigger rate reductions

- Crossing rate
  - 36x36 bunches, 396 ns
  - 1.7 MHz
- Level 1
  - Synchronous, pipelined
  - 40 (17) kHz accept rate
- Level 2
  - Asynchronous, buffered
  - 300 Hz accept rate
- Level 3
  - PC farm
  - 75 Hz accept rate



HRR Halts, Resets and Restarts the L1 Pipeline

The Trigger System Interface

Components

- The Global Level 1 Trigger
- The Trigger Supervisor
- The Trigger Crosspoints
- The Return Crosspoints
- The Scalers

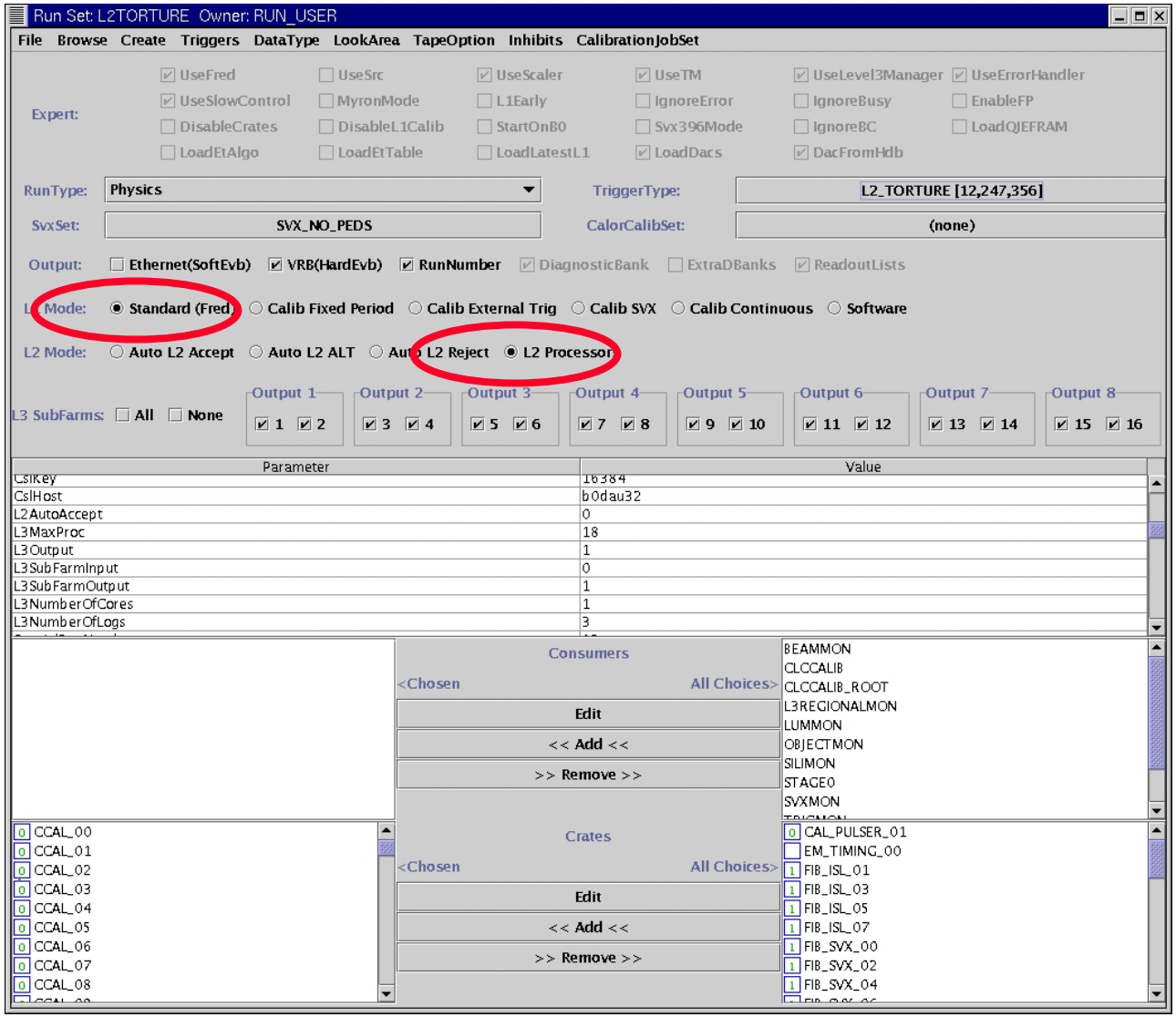
The Global Level 1 Trigger – b011gl00

- a.k.a FRED
- Forms 64 L1 triggers every 132 ns
- Data from calorimeter, muons, tracking, CLC, TOF, diffractive
- Sends preliminary L1 decision to the Trigger Supervisor
- Sends 64 L1 trigger bits to Level 2 crate
- Sends trigger data to scalers for rate accounting
- Ace Monitors trigger rates on “Rates and Deadtimes” GUI
  - Cosmic rate ~ 50 Hz
  - Level 1 design rate = 40 kHz
  - Bunch Crossing rate = 1.7 MHz
- CO checks trigger performance with TrigMon, XMon

The Trigger Supervisor (TS) – b0tsi00

- Controls the synchronous flow of event data from the Front-End crates to the Event Builder (EVB)
- Manages the filling and readout of the four Level 2 buffers
- Receives L1A/R recommendation from FRED
- Sends out the final L1 decision based on L2 buffer availability
- Receives the L2 decision from the L2 (Alpha) crate and sends it to the Front-End crates
- The Trigger Manager process sends TS event data to the EVB
- TS sends Livetime accounting signals to the Scaler crate
- The TS can also control the Front-End independently of the Trigger
  - Auto L1 Accept in “calib continuous” mode
  - L1 Accept based on external calibration signals
  - Auto L2 Accept
- There are 8 Trigger Supervisors

There are many different ways to trigger and readout



1. Standard or Physics
   - Standard (Fred)
   - L2 Processors
   - VRB (HardEvb)

2. Null or DAQ Test
   - Calib Continuous
   - Auto L2 Accept
   - Ethernet (SoftEvb)

3. Other combinations

Note: There are “TS Auto L2 Accept” and “Alpha Auto L2 Accept” modes!

The Trigger Crosspoints (TXPT) – b0tsi01

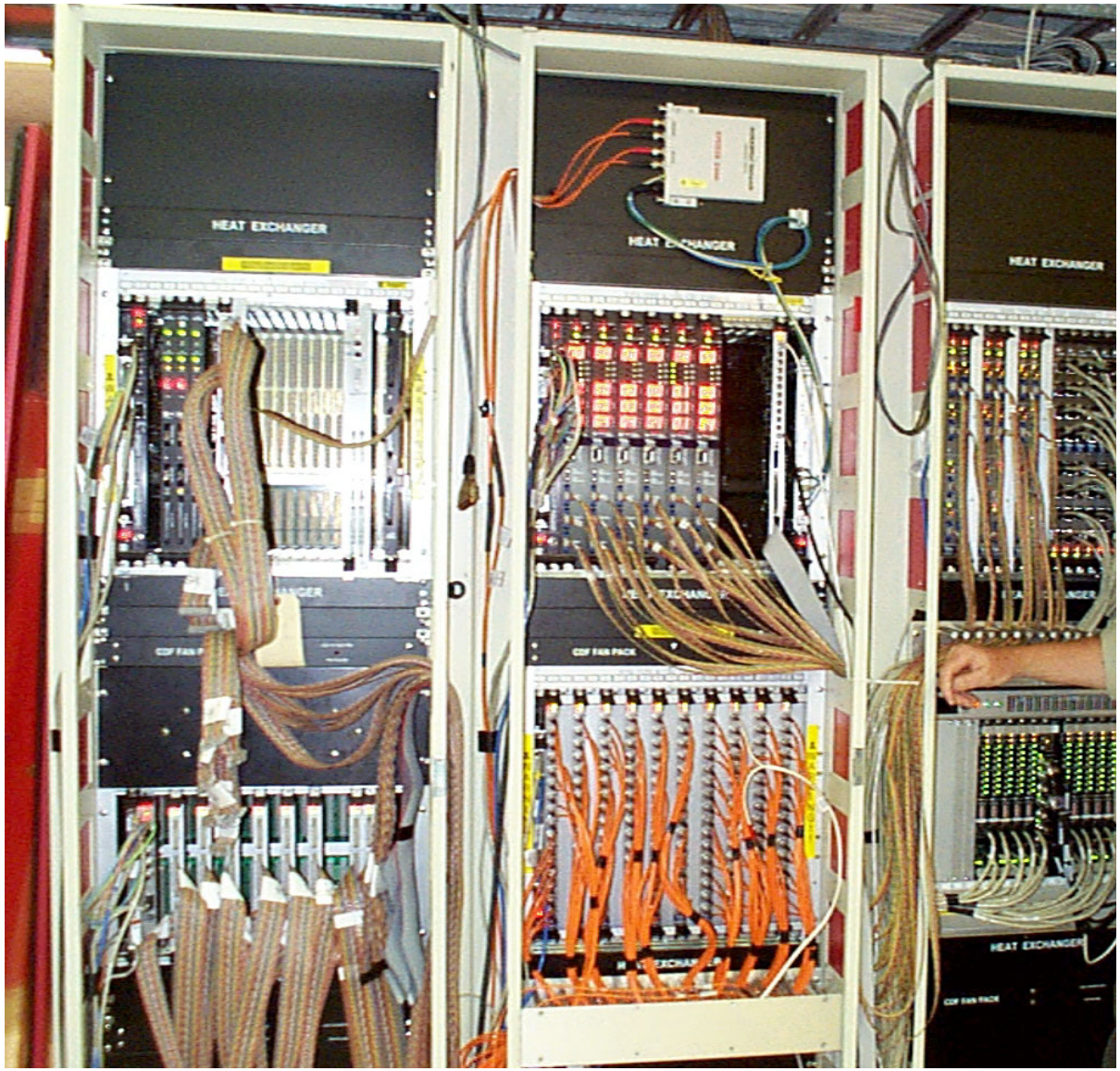
- Routes TS messages (L1A, L2A, HRR) to the Tracers in the Front-End crates
- Responsible for partitioning the detector
- Allows subsets of the ~ 120 Front-End crates to be controlled by different Trigger Supervisors
- There is only one “Physics” partition; I.e. the Trigger cannot be partitioned
- Note: Each crate is always listening to one partition!

The Return Crosspoints (RXPT) – b0tsi02

- Monitors DONE, ERROR, and BUSY signals from the Tracers in the Front-End crates
- DONE de-asserted on receipt of L2 Accept and re-asserted when data readout is complete
- DONE timeout occurs when this take too long
- BUSY signal sent to RXPT if Tracer/VRB is not ready for another L2A
- BUSY timeout indicates problem at the VRB/EVB interface
- ERROR sent to RXPT from the Tracer if something goes wrong in a Front-End crate
- The ERROR feature is not widely used …
- The ACE monitors Return Crosspoint activity on the DAQMon "RXPT" GUI

The Scaler Crate – b0tsi03

- Provides L1 trigger rates from FRED data
- Provides global L1 and L2 accept rates from the TS
- Provides Livetime and Deadtime accounting form the TS
- Information displayed in real time on “Rates and Deadtimes” GUI
- Scaler data also readout on each L2 Accept and sent to Xmon



SCRAMNet to EVB

RXPT (b0tsi02)

CLOCK

FRED (b0l1gl00)

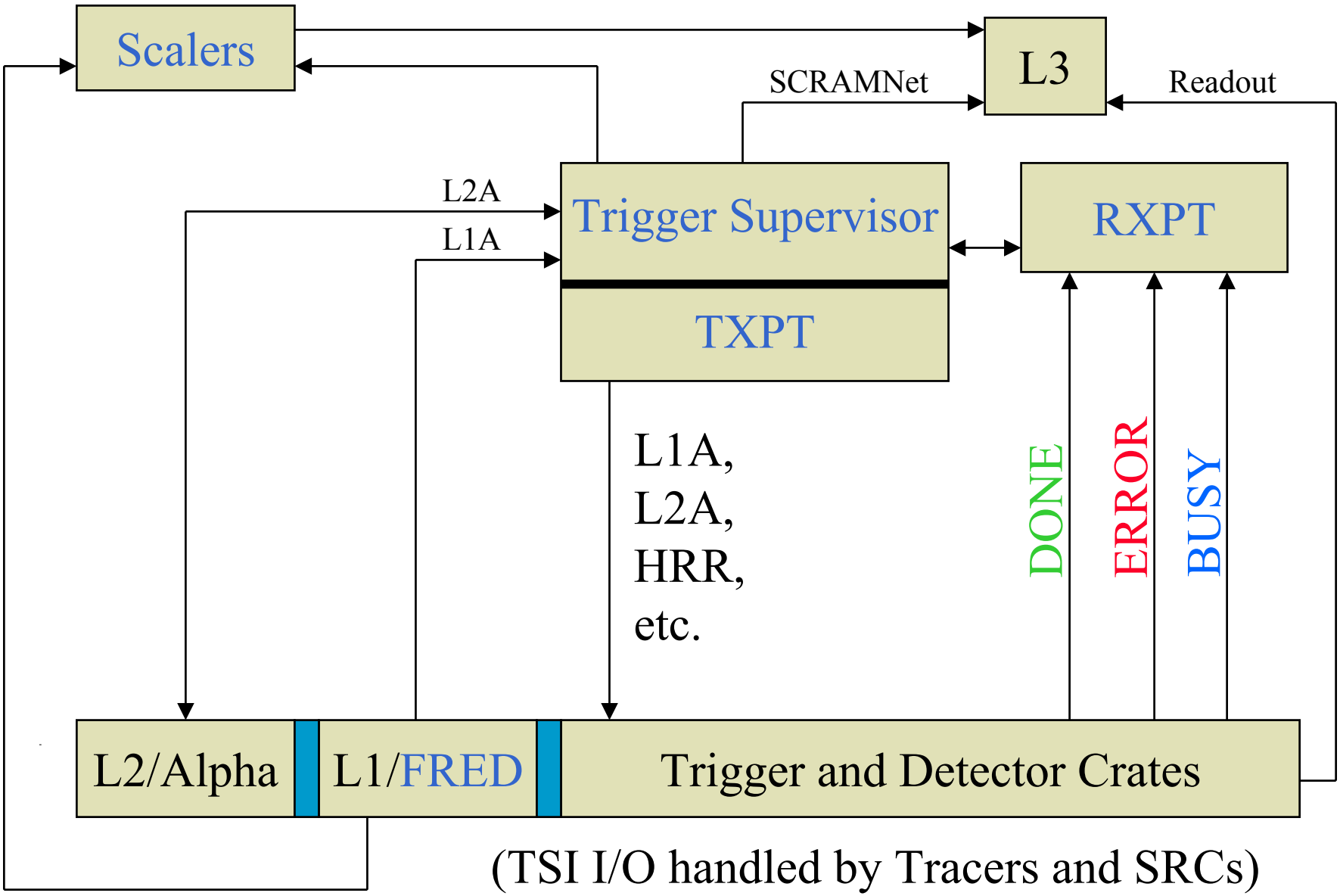
SCALERS (b0tsi03)

TS (b0tsi00)

TXPT (b0tsi01)

The Trigger System Interface

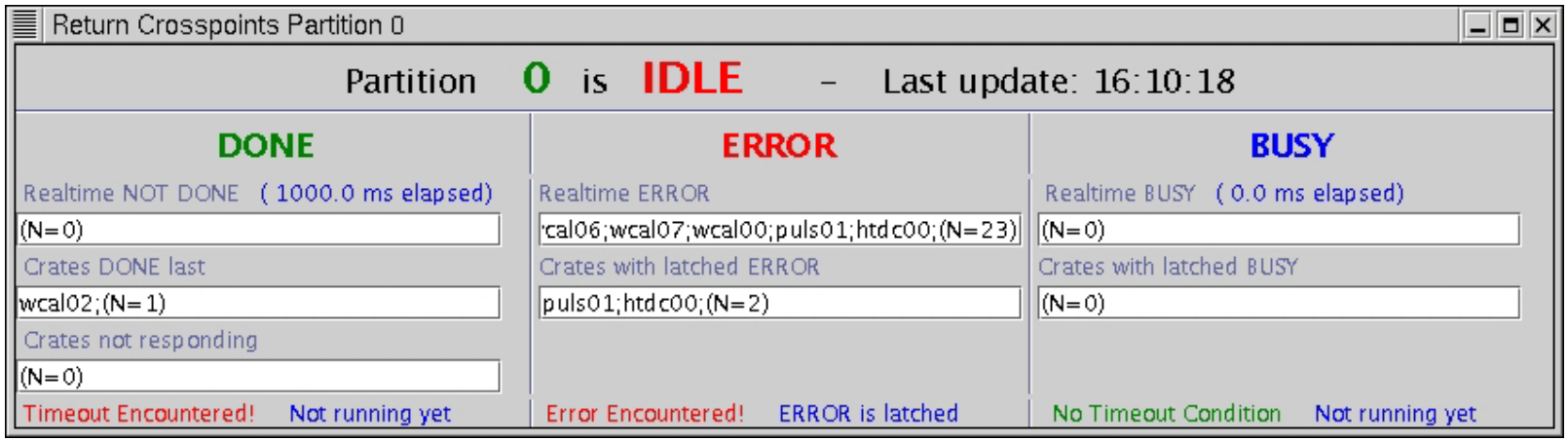
The Trigger System Interface (TSI)



The RXPT Monitor

Available from DAQMON. Click on RXPT and then select the partition.

Front-end crates are usually not the cause of BUSY Deadtime (e.g. svx02, tsi03)



Look here for the offending crate(s) if you have high READOUT Deadtime

Look here when a run fails to start with b0tsi00 going RED and messages like "TS L2 FSM failed to start" . Usually a front-end crate is pulling CDF_ERROR

More on the Scalers

- The Scalers are banks of counters with VME readout.

  These hardware scalers do the TSI accounting
  - Livetime/Deadtime accounting
  - Level 1 trigger rates (GFRED gated)
  - Buffer occupancy, etc.
- There are also “software” scalers
  - Level 1 trigger rates (GLIVE gated)
  - Level 2 trigger rates
  - Level 3 trigger rates

Deadtime

- Deadtime occurs when the Trigger Supervisor must send a Level 1 reject regardless of what the trigger tells it to do
- Deadtime (> 5%) is bad!

Deadtime/Livetime accounting

- Input signals to Deadtime/Livetime accounting include
  - CDF_CLK – the basic unit of time
  - CDF_BC – gate indicating a filled crossing
  - CDF_ABORT – gate marking crossings in the abort gap
  - BUSY – from the VRBs via the Tracer
  - INHIBIT – trigger inhibit
  - TS_RUN – as in Halt/Recover/Run
  - TS_PAUSE – from the PAUSE button on the Run Control GUI
  - L2BF_EMPTY – Internal TS signal marker indicating at least one free buffer

Definition of Deadtime/Livetime signals

- Runtime gate: GRUN = $\overline{TS\_RUN*TS\_PAUSE*CDF\_BC*CDF\_ABORT}$
- Livetime Gate: GLIVE = $\overline{GRUN*L2BF\_EMPTY*INHIBIT}$
- Fredtime Gate: GFRED = $\overline{GRUN*INHIBIT}$

- DEADTIME = RUNTIME - LIVETIME

Accounting signals

- RUNTIME = GRUN*CDF_CLK

  Counts each filled crossing the DAQ is enabled to run
- LIVETIME = GLIVE*CDF_CLK

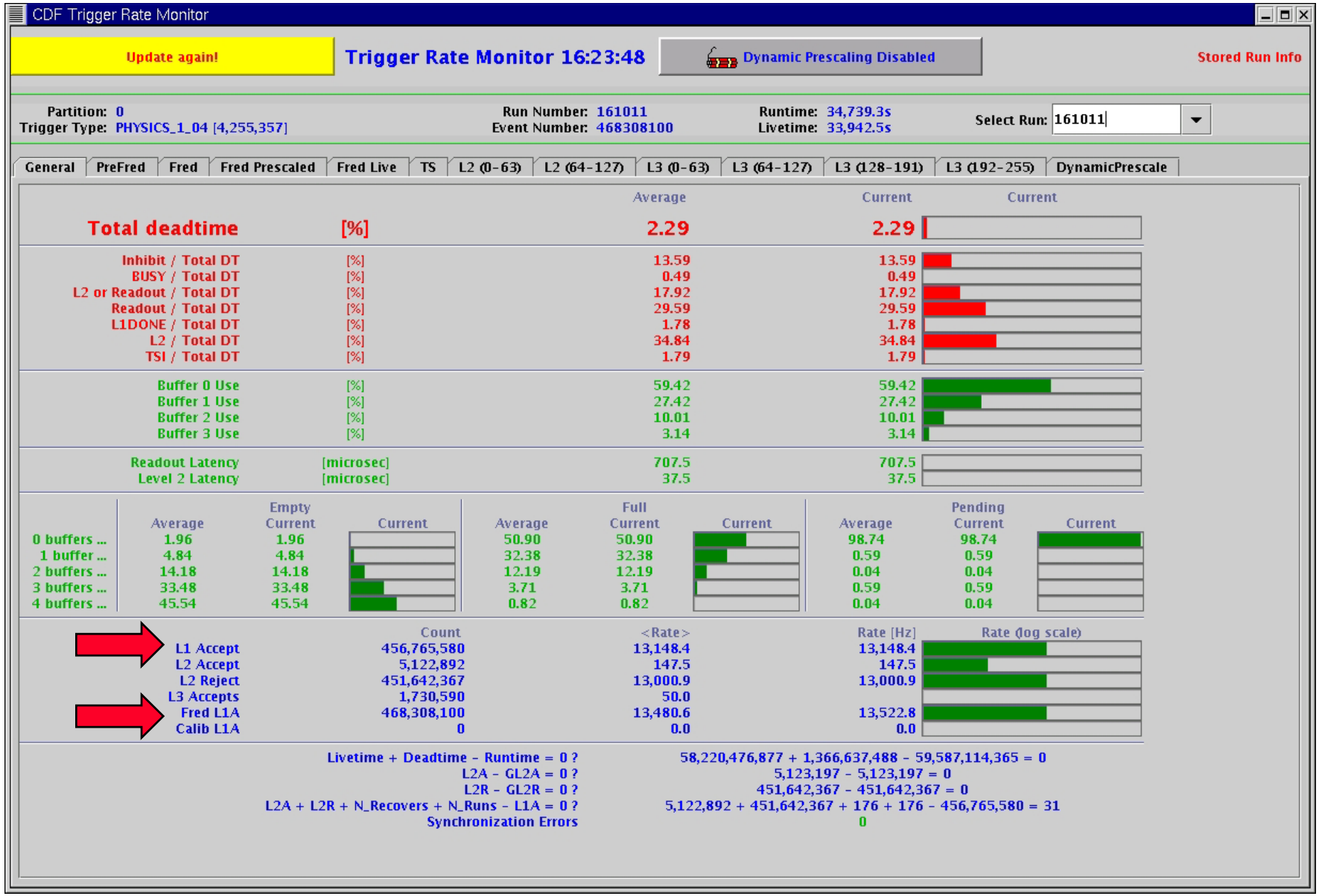
  Counts each filled beam crossing the DAQ is enabled to run and is not forced to send Level 1 rejects

- DEADTIME = RUNTIME - LIVETIME

Sources of Deadtime

- INHIBIT_DEAD: Usually an HV trip
- No free Level 2 buffers
  - BUSY_DEAD: A VRB is filling up. Check EVB status
  - L1DONE_DEAD: Waiting for L1_DONE from SRC. Check Silicon status
  - L2_DEAD: All 4 buffers full. Waiting for L2 decision from Alpha. Page L2 expert.
  - READOUT_DEAD: 4 L2 accepts issued. Front-end crate(s) slow to respond. Find slow crate with RXPT monitor
  - TSI_DEADTIME: Time lost due to TS book-keeping. Very rare. Can occur instead of BUSY deadtime when running without Silicon. Check EVB.
- Level 2 buffers will fill up if the L1 accept rate is too high

The Scaler Monitor – Note distinction between L1A and Fred L1A



The Scaler Monitor

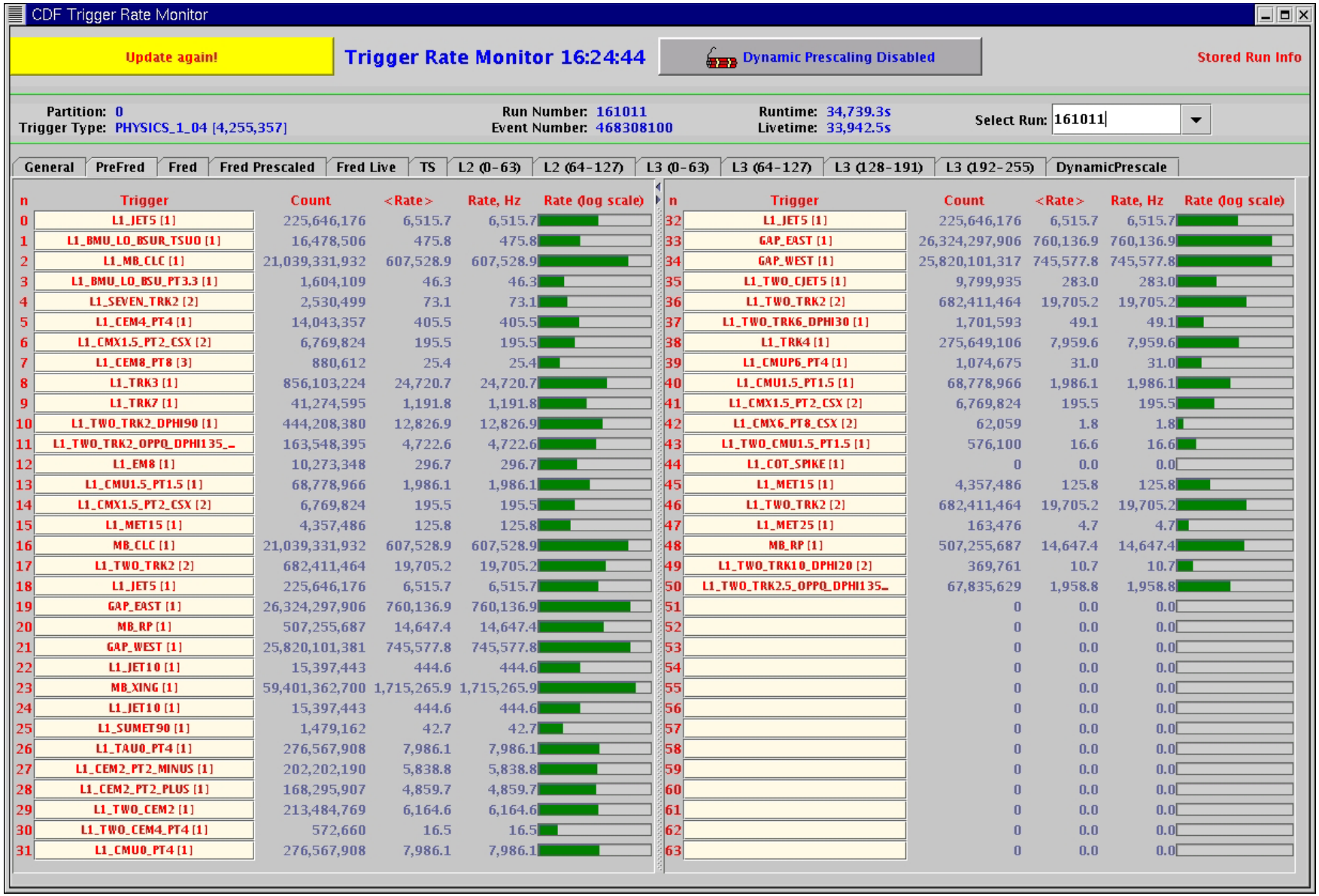
There are two Level 1 rates displayed: “L1 Accept” and “Fred L1A”.
In the limit of 0% Deadtime they should be the same.

Fred L1A is the rate at which the detector/trigger is trying to drive the system. This is the L1A rate to note during a SPIKE run, for example.

The L1 Accept rate is the actual trigger rate seen by the Front-end crates and is governed by L2 buffer availability.

Also note: Even when the Total Deadtime is quite small (1%), the individual contributions to the Deadtime add to 100%.

PreFRED trigger rates



n	Trigger	Count	<Rate>	Rate, Hz	Rate (log scale)
0	L1_JET5 [1]	225,646,176	6,515.7	6,515.7	
1	L1_BMU_LO_BSUR_TSUO [1]	16,478,506	475.8	475.8	
2	L1_MB_CLC [1]	21,039,331,932	607,528.9	607,528.9	
3	L1_BMU_LO_BSU_PT3.3 [1]	1,604,109	46.3	46.3	
4	L1_SEVEN_TRK2 [2]	2,530,499	73.1	73.1	
5	L1_CEM4_PT4 [1]	14,043,357	405.5	405.5	
6	L1_CMX1.5_PT2_CSX [2]	6,769,824	195.5	195.5	
7	L1_CEM8_PT8 [3]	880,612	25.4	25.4	
8	L1_TRK3 [1]	856,103,224	24,720.7	24,720.7	
9	L1_TRK7 [1]	41,274,595	1,191.8	1,191.8	
10	L1_TWO_TRK2_DPHI90 [1]	444,208,380	12,826.9	12,826.9	
11	L1_TWO_TRK2_OPPQ_DPHI135_...	163,548,395	4,722.6	4,722.6	
12	L1_EM8 [1]	10,273,348	296.7	296.7	
13	L1_CMU1.5_PT1.5 [1]	68,778,966	1,986.1	1,986.1	
14	L1_CMX1.5_PT2_CSX [2]	6,769,824	195.5	195.5	
15	L1_MET15 [1]	4,357,486	125.8	125.8	
16	MB_CLC [1]	21,039,331,932	607,528.9	607,528.9	
17	L1_TWO_TRK2 [2]	682,411,464	19,705.2	19,705.2	
18	L1_JET5 [1]	225,646,176	6,515.7	6,515.7	
19	GAP_EAST [1]	26,324,297,906	760,136.9	760,136.9	
20	MB_RP [1]	507,255,687	14,647.4	14,647.4	
21	GAP_WEST [1]	25,820,101,381	745,577.8	745,577.8	
22	L1_JET10 [1]	15,397,443	444.6	444.6	
23	MB_XING [1]	59,401,362,700	1,715,265.9	1,715,265.9	
24	L1_JET10 [1]	15,397,443	444.6	444.6	
25	L1_SUMET90 [1]	1,479,162	42.7	42.7	
26	L1_TAU0_PT4 [1]	276,567,908	7,986.1	7,986.1	
27	L1_CEM2_PT2_MINUS [1]	202,202,190	5,838.8	5,838.8	
28	L1_CEM2_PT2_PLUS [1]	168,295,907	4,859.7	4,859.7	
29	L1_TWO_CEM2 [1]	213,484,769	6,164.6	6,164.6	
30	L1_TWO_CEM4_PT4 [1]	572,660	16.5	16.5	
31	L1_CMU0_PT4 [1]	276,567,908	7,986.1	7,986.1	

n	Trigger	Count	<Rate>	Rate, Hz	Rate (log scale)
32	L1_JET5 [1]	225,646,176	6,515.7	6,515.7	
33	GAP_EAST [1]	26,324,297,906	760,136.9	760,136.9	
34	GAP_WEST [1]	25,820,101,317	745,577.8	745,577.8	
35	L1_TWO_CJET5 [1]	9,799,935	283.0	283.0	
36	L1_TWO_TRK2 [2]	682,411,464	19,705.2	19,705.2	
37	L1_TWO_TRK6_DPHI30 [1]	1,701,593	49.1	49.1	
38	L1_TRK4 [1]	275,649,106	7,959.6	7,959.6	
39	L1_CMUP6_PT4 [1]	1,074,675	31.0	31.0	
40	L1_CMU1.5_PT1.5 [1]	68,778,966	1,986.1	1,986.1	
41	L1_CMX1.5_PT2_CSX [2]	6,769,824	195.5	195.5	
42	L1_CMX6_PT8_CSX [2]	62,059	1.8	1.8	
43	L1_TWO_CMU1.5_PT1.5 [1]	576,100	16.6	16.6	
44	L1_COT_SMKE [1]	0	0.0	0.0	
45	L1_MET15 [1]	4,357,486	125.8	125.8	
46	L1_TWO_TRK2 [2]	682,411,464	19,705.2	19,705.2	
47	L1_MET25 [1]	163,476	4.7	4.7	
48	MB_RP [1]	507,255,687	14,647.4	14,647.4	
49	L1_TWO_TRK10_DPHI20 [2]	369,761	10.7	10.7	
50	L1_TWO_TRK2.5_OPPQ_DPHI135_...	67,835,629	1,958.8	1,958.8	
51		0	0.0	0.0	
52		0	0.0	0.0	
53		0	0.0	0.0	
54		0	0.0	0.0	
55		0	0.0	0.0	
56		0	0.0	0.0	
57		0	0.0	0.0	
58		0	0.0	0.0	
59		0	0.0	0.0	
60		0	0.0	0.0	
61		0	0.0	0.0	
62		0	0.0	0.0	
63		0	0.0	0.0